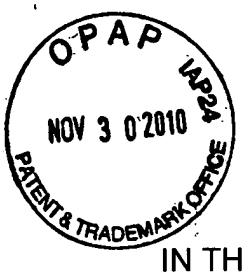

PATENT
Customer No. 22,852
Attorney Docket No. 11368.0001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Qingjiang Ma et al.	)	Group Art Unit: 2611
	)	
Application No.: 10/596,987	)	Examiner: Malek, Leila
	)	
Filed: July 3, 2006	)	
	)	Confirmation No.: 4082
For: SYSTEM AND METHOD FOR CLOCK SIGNAL SYNCHRONIZATION	)	

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

The above-identified application was allowed in the Notice of Allowance mailed on September 2, 2010. Applicants appreciate the notice of allowance. However, Applicants respectfully submit these Comments to address and clarify a statement in the Examiner's reasons for allowance.

In particular, the Examiner stated that "[a]s to claims 11-20, 23-25 and 27-30, a comprehensive search of prior art of record failed to teach either alone or in combination a method/apparatus for synchronizing a clock signal to a data stream by generating a reference signal; generating a digital value equal to a number of cycles of the reference signal in a time duration covering a predetermined number of bit periods in a packet in the data stream; and generating a clock signal synchronized with the data

stream by calculating a number of cycles of the reference signal in a bit period of the data stream from the digital value and the predetermined number, wherein the step of generating a clock signal includes the steps of: setting a count to zero; detecting a change in a bit value in the data stream; in response to a change in the bit value: generating a first edge for a cycle of the clock signal; and setting the count to zero; in response to no change in the bit value: increasing the count by one; in response to the count being equal to the digital value, setting the count to zero; in response to the count being equal to an odd multiple of the digital value divided by two times of the predetermined number, generating a second edge for the cycle of the clock signal; and in response to the count being equal to a multiple of the digital value divided by the predetermined number, generating a third edge for the cycle of the clock signal; and returning to the step of detecting a change in a bit value." Notice of Allowability, page 3 (emphasis omitted). Applicants respectfully point out that the claim elements quoted by the Examiner do not all appear in claims 14-20, 23-25, and 27-30.

Applicants respectfully request that these Comments be entered and any extensions of time required to enter the Comments be granted.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 30, 2010

By: _____

Qingyu Yin
Reg. No. 61,329
(202) 408-4000